	L #	Hits	Search Text	DBs
1	L1	366	multiplier near10 alu near10 shifter	USPAT; US-PGPUB
2	L2	51	1 and sequencer	USPAT; US-PGPUB
3	L4	184	1 and (sequenc$3 near10 instruction) not 2	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030172246 A1	☐	Circular addressing algorithms providing increased compatibility with one or more higher-level programming languages	711/220
2	US 20030172238 A1	☐	Atomically testing and setting or clearing one or more bits stored in a memory location	711/154
3	US 20030172100 A1	☐	Calculating a sum of numbers using an overflow counter in an environment exceeded by the numbers in bit-size	708/513
4	US 20030163500 A1	☐	64-bit scaled sum-of-product operations in a 32-bit environment	708/513
5	US 20030163499 A1	☐	Limiting the valve of a 64-bit number to a maximum value, a minimum value, or both in a 32-bit environment	708/513
6	US 20030140212 A1	☐	Single instruction multiple data array cell	712/22
7	US 20030128748 A1	☐	Path search for CDMA implementation	375/148
8	US 20030028845 A1	☐	High performance turbo and viterbi channel decoding in digital signal processors	714/796
9	US 20030028750 A1	☐	Method and system for digital signal processing in an adaptive computing engine	712/10
10	US 20030014682 A1	☐	Clock generation systems and methods	713/500
11	US 20020116595 A1	☐	Digital signal processor integrated circuit	712/22
12	US 20020116181 A1	☐	Hardware function generator support in a DSP	704/205
13	US 20020089348 A1	☐	Programmable logic integrated circuit devices including dedicated processor components	326/38
14	US 6683804 B1	☐	Read/write memory arrays and methods with predetermined and retrievable latent-state patterns	365/154
15	US 6556324 B1	☐	Device for controlling the beam alignment in satellite laser communications systems	398/129
16	US 6510510 B1	☐	Digital signal processor having distributed register file	712/218
17	US 6385545 B1	☐	Method and apparatus for determining dip angle and horizontal and vertical conductivities	702/10
18	US 6332188 B1	☐	Digital signal processor with bit FIFO	712/204
19	US 6317819 B1	☐	Digital signal processor containing scalar processor and a plurality of vector processors operating from a single instruction	712/22

	Document ID	U	Title	Current OR
20	US 6230278 B1	☐	Microprocessor with functional units that can be selectively coupled	713/324
21	US 6218841 B1	☐	Method and apparatus for determining dip angle, and horizontal and vertical conductivities using multi frequency measurments and a model	324/338
22	US 6163836 A	☐	Processor with programmable addressing modes	712/37
23	US 6112298 A	☐	Method for managing an instruction execution pipeline during debugging of a data processing system	712/227
24	US 6094726 A	☐	Digital signal processor using a reconfigurable array of macrocells	713/400
25	US 6092024 A	☐	Method and apparatus for determining resistivity and dielectric anisotropy parameters of earth formations by using multifrequency and/or multispacing measurements	702/7
26	US 6081885 A	☐	Method and apparatus for halting a processor and providing state visibility on a pipeline phase basis	712/227
27	US 6065106 A	☐	Resuming normal execution by restoring without refetching instructions in multi-word instruction register interrupted by debug instructions loading and processing	712/24
28	US 6061779 A	☐	Digital signal processor having data alignment buffer for performing unaligned data accesses	712/204
29	US 6055649 A	☐	Processor test port with scan chains and data streaming	714/30
30	US 6016555 A	☐	Non-intrusive software breakpoints in a processor instruction execution pipeline	714/35
31	US 5970241 A	☐	Maintaining synchronism between a processor pipeline and subsystem pipelines during debugging of a data processing system	712/227
32	US 5954811 A	☐	Digital signal processor architecture	712/35
33	US 5926644 A	☐	Instruction formats/instruction encoding	712/22
34	US 5896543 A	☐	Digital signal processor architecture	712/35
35	US 5869968 A	☐	Method and apparatus for avoiding mutual coupling between receivers in measurement while drilling	324/338
36	US 5811972 A	☐	Method and apparatus for determining influence of mutual magnetic coupling in electromagnetic propagation tools	324/338
37	US 5752068 A	☐	Mesh parallel computer architecture apparatus and associated methods	712/16
38	US 5717891 A	☐	Digital signal processor with caching of instructions that produce a memory conflict	711/125
39	US 5685005 A	☐	Digital signal processor configured for multiprocessing	712/36
40	US 5682099 A	☐	Method and apparatus for signal bandpass sampling in measurement-while-drilling applications	324/338
41	US 5634076 A	☐	DMA controller responsive to transition of a request signal between first state and second state and maintaining of second state for controlling data transfer	710/22
42	US 5619720 A	☐	Digital signal processor having link ports for point-to-point communication	712/38

	Document ID	U	Title	Current OR
43	US 5617058 A	☐	Digital signal processing for linearization of small input signals to a tri-state power switch	330/10
44	US 5611075 A	☐	Bus architecture for digital signal processor allowing time multiplexed access to memory banks	711/153
45	US 5590356 A	☐	Mesh parallel computer architecture apparatus and associated methods	712/31
46	US 5574374 A	☐	Method and apparatus for interrogating a borehole and surrounding formation utilizing digitally controlled oscillators	324/338
47	US 5379388 A	☐	Digital signal processing apparatus with sequencer designating program routines	712/248
48	US 5365465 A	☐	Floating point to logarithm converter	708/204
49	US 5233698 A	☐	Method for operating data processors	713/601
50	US 5155817 A	☐	Microprocessor	712/218
51	US 5062041 A	☐	Processor/coprocessor interface apparatus including microinstruction clock synchronization	712/221

	Document ID	U	Title	Current OR
1	US 20040039952 A1	☐	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
2	US 20040039900 A1	☒	Processor, program conversion apparatus, program conversion method, and computer program	712/234
3	US 20040015680 A1	☒	Data processor for modifying and executing operation of instruction code	712/226
4	US 20040010321 A1	☒	Data processor and program	700/2
5	US 20030226002 A1	☒	Devices, systems and methods for conditional instructions notice	712/234
6	US 20030200423 A1	☒	Repeat block with zero cycle overhead nesting	712/228
7	US 20030196072 A1	☒	Digital signal processor architecture for high computation speed	712/32
8	US 20030196058 A1	☒	Memory system for supporting multiple parallel accesses at very high frequencies	711/169
9	US 20030163679 A1	☒	Method and apparatus for loop buffering digital signal processing instructions	712/241
10	US 20030056134 A1	☒	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
11	US 20030056088 A1	☒	Processor, compiler and compilation method	712/214
12	US 20030023833 A1	☒	Apparatus and systems for dyadic digital signal processing instructions	712/35
13	US 20030023832 A1	☒	Instruction set architecture for signal processors	712/35
14	US 20030018882 A1	☒	Dyadic DSP instructions for digital signal processors	712/35
15	US 20030018881 A1	☒	Methods of dyadic DSP instruction operation	712/35
16	US 20020188824 A1	☒	Method and apparatus for instruction set architecture to perform primary and shadow digital signal processing sub-instructions simultaneously	712/35
17	US 20020184472 A1	☒	Microcomputer	712/33

	Document ID	U	Title	Current OR
18	US 20020178347 A1	☒	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
19	US 20020138715 A1	☒	Microprocessor executing data transfer between memory and register and data transfer between registers in response to single push/pop instruction	712/225
20	US 20020120830 A1	☒	Data processor assigning the same operation code to multiple operations	712/209
21	US 20020116186 A1	☒	Voice activity detector for integrated telecommunications processing	704/233
22	US 20020112144 A1	☒	APPARATUS AND METHOD FOR CODE-ENHANCED PERFORMANCE IN A DIGITAL SIGNAL PROCESSING UNIT	712/29
23	US 20020076034 A1	☒	Tone detection for integrated telecommunications processing	379/390.02
24	US 20020064139 A1	☒	Network echo canceller for integrated telecommunications processing	370/289
25	US 20020041626 A1	☒	Media processing apparatus which operates at high efficiency	375/240
26	US 20020026545 A1	☒	Data processing apparatus of high speed process using memory of low speed and low power consumption	710/56
27	US 20020002670 A1	☒	DATA PROCESSING DEVICE	712/245
28	US 20010010072 A1	☒	Instruction translator translating non-native instructions for a processor into native instructions therefor, instruction memory with such translator, and data processing apparatus using them	712/209
29	US 6671797 B1	☒	Microprocessor with expand instruction for forming a mask from one bit	712/224
30	US 6658578 B1	☒	Microprocessors	713/324
31	US 6643768 B2	☒	Dyadic DSP instruction processor with main and sub-operation functional blocks selected from each set of multiplier and adder	712/221
32	US 6631461 B2	☒	Dyadic DSP instructions for digital signal processors	712/221
33	US 6615339 B1	☒	VLIW processor accepting branching to any instruction in an instruction word set to be executed consecutively	712/24
34	US 6598155 B1	☒	Method and apparatus for loop buffering digital signal processing instructions	712/241
35	US 6594728 B1	☒	Cache memory with dual-way arrays and multiplexed parallel output	711/127
36	US 6574724 B1	☒	Microprocessor with non-aligned scaled and unscaled addressing	711/220

	Document ID	U	Title	Current OR
37	US 6567910 B2	☒	Digital signal processing unit with emulation circuitry and debug interrupt enable register indicating serviceable time-critical interrupts during real-time emulation mode	712/227
38	US 6550000 B1	☒	Processor to execute in parallel plurality of instructions using plurality of functional units, and instruction allocation controller	712/215
39	US 6539467 B1	☒	Microprocessor with non-aligned memory access	711/219
40	US 6470376 B1	☒	Processor capable of efficiently executing many asynchronous event tasks	718/108
41	US 6463520 B1	☒	Processor for executing instruction codes of two different lengths and device for inputting the instruction codes	712/205
42	US 6446195 B1	☒	Dyadic operations instruction processor with configurable functional blocks	712/221
43	US 6434690 B1	☒	Microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CUP-type instructions	712/35
44	US 6412064 B1	☒	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
45	US 6408376 B1	☒	Method and apparatus for instruction set architecture to perform primary and shadow digital signal processing sub-instructions simultaneously	712/36
46	US 6405302 B1	☒	Microcomputer	712/35
47	US 6374346 B1	☒	Processor with conditional execution of every instruction	712/221
48	US 6341324 B1	☒	Exception processing in superscalar microprocessor	710/260
49	US 6334181 B1	☒	DSP with wait state registers having at least two portions	712/38
50	US 6327631 B1	☒	Signal processing apparatus	709/400
51	US 6324639 B1	☒	Instruction converting apparatus using parallel execution code	712/212
52	US 6311264 B1	☒	Digital signal processor with wait state register	712/38
53	US 6310921 B1	☒	Media processing apparatus which operates at high efficiency	375/240.26
54	US 6301655 B1	☒	Exception processing in asynchronous processor	712/244
55	US 6292881 B1	☒	Microprocessor, operation process execution method and recording medium	712/41
56	US 6282708 B1	☒	Method and processor for structuring a multi-instruction computer program in an internal directed acyclic graph	717/156
57	US 6266755 B1	☒	Translation lookaside buffer with virtual address conflict prevention	711/210
58	US 6263419 B1	☒	Integrated circuit with wait state registers	712/38
59	US 6263418 B1	☒	Process of operating a microprocessor to use wait state numbers	712/38

	Document ID	U	Title	Current OR
60	US 6260088 B1	☒	Single integrated circuit embodying a risc processor and a digital signal processor	710/100
61	US 6253307 B1	☒	Data processing device with mask and status bits for selecting a set of status conditions	712/209
62	US 6249860 B1	☒	System with wait state registers	712/38
63	US 6247111 B1	☒	System with wait state register	712/38
64	US 6243801 B1	☒	System with wait state registers	712/38
65	US 6243735 B1	☒	Microcontroller, data processing system and task switching control method	718/102
66	US 6240505 B1	☒	System with wait state registers	712/38
67	US 6240504 B1	☒	Process of operating a microprocessor to change wait states	712/38
68	US 6216200 B1	☒	Address queue	711/100
69	US 6209079 B1	☒	Processor for executing instruction codes of two different lengths and device for inputting the instruction codes	712/210
70	US 6178492 B1	☒	Data processor capable of executing two instructions having operand interference at high speed in parallel	712/23
71	US 6167509 A	☒	Branch performance in high speed processor	712/237
72	US 6134578 A	☒	Data processing device and method of operation with context switching	718/100
73	US 6131157 A	☒	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
74	US 6128725 A	☒	Microprocessor with an instruction for setting or clearing a bit field	712/200
75	US 6124724 A	☒	Computation using codes for controlling configurable computational circuit	712/32
76	US 6112289 A	☒	Data processor	712/23
77	US 6108765 A	☒	Device for digital signal processing	712/32
78	US 6092184 A	☒	Parallel processing of pipelined instructions having register dependencies	712/218
79	US 6076158 A	☒	Branch prediction in high-performance processor	712/230
80	US 6070003 A	☒	System and method of memory access in apparatus having plural processors and plural memories	710/317
81	US 6055628 A	☒	Microprocessor with a nestable delayed branch instruction without branch related pipeline interlocks	712/235
82	US 6038584 A	☒	Synchronized MIMD multi-processing system and method of operation	709/248

	Document ID	U	Title	Current OR
83	US 6021265 A	☒	Interoperability with multiple instruction sets	712/209
84	US 6003129 A	☒	System and method for handling interrupt and exception events in an asymmetric multiprocessor architecture	712/244
85	US 6000025 A	☒	Method of signal processing by contemporaneous operation of ALU and transfer of data	712/32
86	US 5996058 A	☒	System and method for handling software interrupts with argument passing	712/31
87	US 5995746 A	☒	Byte-compare operation for high-performance processor	712/220
88	US 5960209 A	☒	Scaleable digital signal processor with parallel architecture	712/1
89	US 5946483 A	☒	Devices, systems and methods for conditional instructions	712/223
90	US 5933624 A	☒	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors while one processor services an interrupt	709/400
91	US 5907714 A	☒	Method for pipelined data processing with conditioning instructions for controlling execution of instructions without pipeline flushing	712/23
92	US 5898878 A	☒	Data processing system having capability to interpolate processing coefficients	710/260
93	US 5892938 A	☒	Interactive interface system	710/8
94	US 5881272 A	☒	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors on write to program counter of one processor	709/400
95	US 5881077 A	☒	Data processing system	714/800
96	US 5867726 A	☒	Microcomputer	712/32
97	US 5854907 A	☒	Microcomputer for digital signal processing having on-chip memory and external memory access	710/100
98	US 5829054 A	☒	Devices and systems with parallel logic unit operable on data memory locations	711/202
99	US 5828896 A	☒	Microcomputer system for digital signal processing	712/33
100	US 5828577 A	☒	Devices and systems with protective terminal configuration, and methods	716/4
101	US 5826111 A	☒	Modem employing digital signal processor	710/69
102	US 5826055 A	☒	System and method for retiring instructions in a superscalar microprocessor	712/218
103	US 5809288 A	☒	Synchronized MIMD multi-processing system and method inhibiting instruction fetch on memory access stall	709/400
104	US 5802385 A	☒	Array processing system with each processor including router and which selectively delays input/output of individual processors in response delay instructions	712/16
105	US 5778423 A	☒	Prefetch instruction for improving performance in reduced instruction set processor	711/118

	Document ID	U	Title	Current OR
106	US 5777885 A	☒	Devices and systems with protective terminal configuration, and methods	716/1
107	US 5768609 A	☒	Reduced area of crossbar and method of operation	712/11
108	US 5765219 A	☒	Apparatus and method for incrementally accessing a system memory	711/220
109	US 5765013 A	☒	Digital signal processor	712/17
110	US 5764943 A	☒	Data path circuitry for processor having multiple instruction pipelines	712/218
111	US 5758195 A	☒	Register to memory data transfers with field extraction and zero/sign extension based upon size and mode data corresponding to employed address register	712/300
112	US 5758115 A	☒	Interoperability with multiple instruction sets	712/209
113	US 5758112 A	☒	Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction	712/217
114	US 5752073 A	☒	Digital signal processor architecture	712/35
115	US 5742780 A	☒	Dual pipeline superscalar reduced instruction set computer system architecture	712/206
116	US 5740449 A	☒	Method and apparatus for managing interrupts in a data processing system	710/260
117	US 5724248 A	☒	Devices and systems with protective terminal configuration, and methods	716/4
118	US 5717946 A	☒	Data processor	712/225
119	US 5696913 A	☒	Unique processor identifier in a multi-processing system having plural memories with a unified address space corresponding to each processor	710/317
120	US 5684435 A	☒	Analog waveform communications reduced instruction set processor	332/117
121	US 5652910 A	☒	Devices and systems with conditional instructions	712/218
122	US 5625838 A	☒	Microcomputer system for digital signal processing	712/32
123	US 5617574 A	☒	Devices, systems and methods for conditional instructions	712/200
124	US 5615383 A	☒	Microcomputer system for digital signal processing	712/43
125	US 5613146 A	☒	Reconfigurable SIMD/MIMD processor using switch matrix to allow access to a parameter memory by any of the plurality of processors	712/20
126	US 5606520 A	☒	Address generator with controllable modulo power of two addressing capability	708/491
127	US 5603047 A	☒	Superscalar microprocessor architecture	712/23
128	US 5592405 A	☒	Multiple operations employing divided arithmetic logic unit and multiple flags register	708/518

	Document ID	U	Title	Current OR
129	US 5586275 A	☒	Devices and systems with parallel logic unit operable on data memory locations, and methods	712/223
130	US 5583767 A	☒	Devices and systems with parallel logic unit, and methods notice	701/1
131	US 5581792 A	☒	Microcomputer system for digital signal processing having external peripheral and memory access	710/52
132	US 5579497 A	☒	Devices and systems with parallel logic unit, and methods	375/222
133	US 5579218 A	☒	Devices and systems with parallel logic unit, and methods	700/1
134	US 5568624 A	☒	Byte-compare operation for high-performance processor	712/223
135	US 5550993 A	☒	Data processor with sets of two registers where both registers receive identical information and when context changes in one register the other register remains unchanged	712/229
136	US 5522083 A	☒	Reconfigurable multi-processor operating in SIMD mode with one processor fetching instructions for use by remaining processors	712/22
137	US 5517436 A	☒	Digital signal processor for audio applications	708/524
138	US 5471592 A	☒	Multi-processor with crossbar link of processors and memories and method of operation	709/213
139	US 5469551 A	☒	Method and apparatus for eliminating branches using conditional move instructions	712/239
140	US 5454091 A	☒	Virtual to physical address translation scheme with granularity hint for identifying subsequent pages to be accessed	711/203
141	US 5450553 A	☒	Digital signal processor including address generation by execute/stop instruction designated	711/214
142	US 5410682 A	☒	In-register data manipulation for unaligned byte write using data shift in reduced instruction set processor	712/300
143	US 5410649 A	☒	Imaging computer system and network	345/505
144	US 5371896 A	☒	Multi-processor having control over synchronization of processors in mind mode and method of operation	712/20
145	US 5367705 A	☒	In-register data manipulation using data shift in reduced instruction set processor	712/41
146	US 5349687 A	☒	Speech recognition system having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	704/231
147	US 5339447 A	☒	Ones counting circuit, utilizing a matrix of interconnected half-adders, for counting the number of ones in a binary string of image data	377/82
148	US 5319792 A	☒	Modem having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
149	US 5319789 A	☒	Electromechanical apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228
150	US 5313648 A	☒	Signal processing apparatus having first and second registers enabling both to concurrently receive identical information in one context and disabling one to retain the information in a next context	712/228

	Document ID	U	Title	Current OR
151	US 52414 92 A	☒	Apparatus for performing multiply and accumulate instructions with reduced power and a method therefor	708/523
152	US 52396 54 A	☒	Dual mode SIMD/MIMD processor providing reuse of MIMD instruction memories as data memories when operating in SIMD mode	712/20
153	US 52333 35 A	☒	Symbol/raster generator for CRT display	345/17
154	US 52261 25 A	☒	Switch matrix having integrated crosspoint logic and method of operation	710/317
155	US 52187 10 A	☒	Audio signal processing system having independent and distinct data buses for concurrently transferring audio signal data to provide acoustic control	704/278
156	US 52127 77 A	☒	Multi-processor reconfigurable in single instruction multiple data (SIMD) and multiple instruction multiple data (MIMD) modes and method of operation	712/229
157	US 51971 40 A	☒	Sliced addressing multi-processor and method of operation	711/220
158	US 51931 67 A	☒	Ensuring data integrity by locked-load and conditional-store operations in a multiprocessor system	711/163
159	US 51558 12 A	☒	Devices and method for generating and using systems, software waitstates on address boundaries in data processing	710/59
160	US 51426 77 A	☒	Context switching devices, systems and methods	718/108
161	US 51366 64 A	☒	Pixel rendering	382/304
162	US 51288 90 A	☒	Apparatus for performing multiplications with reduced power and a method therefor	708/625
163	US 50724 18 A	☒	Series maxium/minimum function computing devices, systems and methods	708/207
164	US 50654 33 A	☒	Audio signal data processing system	381/63
165	US 47137 49 A	☒	Microprocessor with repeat instruction	712/241
166	US 47137 48 A	☒	Microprocessor with block move instruction	712/225
167	US 46775 86 A	☒	Microcomputer device having test mode substituting external RAM for internal RAM	714/27
168	US 46384 51 A	☒	Microprocessor system with programmable interface	710/69
169	US 46086 34 A	☒	Microcomputer with offset in store-accumulator operations	712/221
170	US 45861 31 A	☒	Microcomputer having data move circuits for within-memory shift of data words	712/221
171	US 45772 82 A	☒	Microcomputer system for digital signal processing	712/33
172	US 45582 32 A	☒	Level detector circuit for microcomputer devices	327/78
173	US 45382 39 A	☒	High-speed multiplier for microcomputer used in digital signal processing system	708/627

	Document ID	U	Title	Current OR
174	US 4533992 A	☒	Microcomputer having shifter in ALU input	712/42
175	US 4528625 A	☒	Input/output instruction execution in microcomputer	712/225
176	US 4519031 A	☒	Microcomputer with accumulator saturation upon overflow	712/32
177	US 4514805 A	☒	Interrupt operation in systems emulator mode for microcomputer	710/261
178	US 4514801 A	☒	Microcomputer with table-read and table-write instructions	712/205
179	US 4507727 A	☒	Microcomputer with ROM test mode of operation	712/33
180	US 4506322 A	☒	Read/write memory cell for microcomputer	711/169
181	US 4503500 A	☒	Microcomputer with bus interchange module	712/33
182	US 4498135 A	☒	Microcomputer with accumulator addressing	712/33
183	US 4494187 A	☒	Microcomputer with high speed program memory	712/37
184	US 4491910 A	☐	Microcomputer having data shift within memory	712/42